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Application No. 10/615,601

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GOVERNMENT OF INDIA
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PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***725/Del/02*** *dated* ***8th July 2002.***

Witness my hand this 27th Day of June 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

0725/02

FORM 1

THE PATENTS ACT, 1970

(39 of 1970)

APPLICATION FOR GRANT OF A PATENT

(See Sections 5(2), 7, 54 and 135)

1. I/We,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare -

(a) that I am/we re in possession of an invention titled *"Improved Binary Decoders In Electronic Integrated Circuits."*

(b) that the ~~provisional~~/ complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) LAL Abhishek, an Indian citizen, of House no. 254, Sector 10, Faridabad 121 006, Haryana, India.

4. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

ORIGINAL

9. Following declaration was given by the inventor(s) ~~or applicant(s) in the convention country~~:

I/we are the true and first inventors for this invention ~~or are and the applicant(s) in the convention country~~ declare that the applicant(s) herein is/are my/our assignee or legal representative

LAL Abhishek

Date: 8th July, 2002

10. that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to the grant of patent to me/us on this application.

11. Followings are the attachment with the application:

(a) ~~provisional /~~ complete specification (3 copies)

(b) Form 1 (in triplicate)

(c) Formal Drawings (3 copies)

(d) Statement and Undertaking on Form 3

(e) Fee Rs. 5000.00 In cash/cheque/bank draft bearing no. , dated 8th July, 2002 on Citibank Bank.

I/we request that a patent may be granted to me/us for the said invention.

Dated this 8th day of July, 2002

of Anand And Anand Advocates
Attorney for the Applicant

To
The Controller of Patents
The Patent Office, Delhi

Form 2

THE PATENTS ACT, 1970

COMPLETE SPECIFICATION

[See Section 10]

"IMPROVED BINARY DECODERS IN ELECTRONIC INTEGRATED CIRCUITS"

STMicroelectronics Pvt. Ltd., *Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 301, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed.

IMPROVED BINARY DECODERS IN ELECTRONIC INTEGRATED CIRCUITS

Field of the Invention:

This invention relates to electronic integrated circuits. In particular it relates to an improved binary decoders in integrated circuits.

Background of the Invention:

A binary decoder is a circuit that enables a single selected digital output from a defined set of digital outputs, based on an input binary value. The decoder produces an output signal on the single output that matches the input binary value. Binary decoders are essentially combinatorial logic circuits formed by an arrangement of logic gates. A binary decoder having an input value "n" bits is required to have "2^n" outputs one of which corresponds with the n-bit value applied at the input. Binary decoders are widely used for performing selection functions where any single device or any single set of devices are required to be selected or enabled from a defined collection of devices or defined collection of device sets. A typical application is in selecting a row of memory cells in a memory device. Another typical application is in selecting a single IO device from a collection of IO devices in an electronic circuit.

A 2-to-4 decoder implementation according to the known art requires 16 transistors covering four different circuits, one for each combination of the input. At the same time each input signal is required to drive four GATE loads. Similarly, a 3-to-8 decoder requires as many as 32 transistors covering 8 different circuits, one for each combination of inputs, with each input having to drive 4 gate loads. This manner of implementation results in a bulky and expensive circuit requiring an undesirably large chip area. The capacitive loading on the input signals reduces the speed of the operation of the device.

SUMMARY OF THE INVENTION

The object of this invention is to provide binary decoders requiring fewer transistors.

Another object of this invention is to provide decoders with reduced loading on input signals.

Yet another object of this invention is to provide decoders with reduced size.

Further object of this invention is to provide decoders with reduced power consumption.

Yet another object of this invention is to provide decoders with reduced delay.

Another object of this invention is to provide cost-effective decoders.

To achieve these and other objects, this invention provides an improved binary decoder incorporating a selection circuit that activates a selected output corresponding to the input binary value, and a deselecting circuit coupled to each output that deactivates all other outputs when the selected output is activated. The deselecting circuit arrangement has a single input connected to the selected output and a plurality of outputs each of which is connected to one of the remaining outputs and forces them to the inactive state whenever the selected output is activated.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in accordance with the accompanying drawings:

Figure 1 shows the schematic diagram of a conventional 2-to-4 decoder, which provides an active low output for an input = A'.B'.

Figure 2 shows the schematic diagram of a conventional 2-to-4 decoder, which provides an active low output for an input = A'.B.

Figure 3 shows the schematic diagram of a conventional 2-to-4 decoder, which provides an active low output for an input = A.B'.

Figure 4 shows the schematic diagram of a conventional 2-to-4 decoder, which provides an active low output for an input = A.B.

Figure 5 shows the schematic circuit diagram of a 2-to-4 decoder according to this invention, which provides an active low output for an input = A'. B' and A.B'.

Figure 6 shows the schematic circuit diagram of a 2-to-4 decoder according to this invention, which provides an active low output for an input = A'.B and A.B.

Figure 7 shows the schematic circuit diagram of a 3-to-8 decoder according to this invention, which provides an active low output for an input = A'.B'.C' and A.B'.C'.

Figure 8 shows the schematic circuit diagram of a 3-to-8 decoder according to this invention, which provides an active low output for an input = A'.B'.C and A.B'.C.

Figure 9 shows the schematic circuit diagram of a 3-to-8 decoder according to this invention, which provides an active low output for an input = A'.B.C' and A.BC'.

Figure 10 shows the schematic circuit diagram of a 3-to-8 decoder according to this invention, which provides an active low output for an input = A'.B.C and A.B.C.

DETAILED DESCRIPTION

Figure 1 shows one circuit of a conventional 2-to-4 decoder, corresponding to a single combination of the inputs = A'.B'. The output **Y0** is set to active low whenever this combination is true. When A = 0, and B = 0 transistors **1.3, 1.4** conduct and pull output **Y0** to 0. For any other condition **Y0** is set to HIGH.

Figure 2 shows another circuit of a conventional 2-to-4 decoder, corresponding to another single combination of the inputs = A'.B. The output **Y1** is set to active low whenever this combination is true. When A = 0, and B = 1 transistors **2.3, 2.4** conduct and pull **Y1** to 0. In any other condition **Y1** is set to HIGH.

Figure 3 shows another circuit of a conventional 2-to-4 decoder, corresponding to the combination of the inputs = A'.B, The output **Y2** is set to active low whenever this combination is true. When inputs A = 1, B = 0 transistors **3.3, 3.4** conduct and pull **Y2** to 0. In any other condition **Y2** is set to HIGH.

Figure 4 shows another circuit of a conventional 2-to-4 decoder, corresponding to a combination of inputs = A B, The output **Y3** is set to active low whenever this combination is true. As shown, when A = 1 and B = 1 transistors **4.3, 4.4** conduct and pull **Y3** to '0'. In any other condition **Y3** is set to HIGH.

Figure 5 shows a schematic circuit diagram for a 2-to-4 decoder in accordance with the invention. The selected output is set active low when the input = A'.B' and A.B'. When A = 0 and B = 0, transistor **5.6** conducts and pulls **Y0** LOW. This causes transistor **5.2** to conduct pulling **Y2** HIGH. Similarly, when the inputs are A = 1, B = 0, transistor **5.3** is in conduction pulling **Y2** LOW thereby causing transistor **5.4** to conduct and pull **Y0** HIGH

Figure 6 shows a schematic diagram of a 2-to-4 decoder in accordance with the invention. for the case when the inputs A'.B' and A'.B. When the inputs are A = 0, B = 1, transistors **6.6** is in conducting state and pulls **Y1** to LOW. This causes transistor **6.2** to conduct pulling **Y3** HIGH. Similarly, when the inputs are A = 1, B = 1, transistor **6.3** is in conducting state and pulls **Y3** to LOW. This results in transistor **6.4** conducting and pulling **Y1** HIGH.

Figure 7 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. for the case when the inputs are A'.B'.C' and A.B'.C'. When the inputs are A = 0, B = 0, C = 0 transistors **7.8** and **7.9** are in conduction pulling **Y0** LOW. This sets transistor **7.3** conducting pulling **Y4** HIGH. Similarly, when the inputs are A = 1, B = 0, C = 0 transistors **7.4, 7.9** are in conduction **Y4** is pulled LOW. This sets transistor **7.5** conducting pulling **Y0** HIGH.

Figure 8 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. for the case when the inputs are A'.B'.C and A.B'.C. When the inputs are A = 0, B = 0, C = 1 transistors **8.8, 8.9** are in conduction and pull **Y1** LOW. This sets transistor **8.3** conducting

pulling **Y5** HIGH. When the inputs are A = 1, B = 0, C = 1 transistors **8.4, 8.9** are in conducting state pulling **Y5** LOW. This sets transistor **8.5** conducting pulling **Y1** HIGH.

Figure 9 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. for the case when the inputs are A'.B.C' and A.B.C'. When the inputs are A = 0, B = 1, C = 0 transistors **9.8, 9.9** are in conduction pulling **Y2** LOW. This sets transistor **9.3** conducting pulling **Y6** HIGH. Similarly, when the inputs are A = 1, B = 1, C = 0 transistors **9.4, 9.9** are in conducting state pulling **Y6** LOW. This sets transistor **9.5** conducting pulling **Y2** HIGH.

Figure 10 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. for the case when the inputs are A'.B.C and A.B.C. When the inputs are A = 0, B = 1, C = 1 transistors **10.8, 10.9** are in conducting state pulling **Y3** LOW. This sets transistor **10.3** conducting pulling **Y7** HIGH. Similarly, when the inputs are A = 1, B = 1, C = 1 transistors **10.4, 10.9** are in conduction pulling **Y7** LOW. This sets transistor **10.5** conducting pulling **Y3** HIGH.

Though the invention has been discussed for "active low" outputs, with only two output pairs in a circuit and for a limited number of input circuits it will be obvious to a person with ordinary skill in the art that it is possible to implement it for other requirements with minor alterations or extensions. The present invention realizes decoders with reduced number of transistors compared to conventional implementations e.g. for realizing a 2-to-4 decoder, the current invention requires 12 transistors as compared to 16 in the conventional scheme. The reduction in the number of transistors increases for larger decoders. For a 3 x 8 decoder the reduction is 12 transistors, while for a 4 x 16 decoder the reduction 32 transistors and so on.

In order to reduce the number of transistors and to reduce the loading on the input signals and hence to increase the speed of operation of the device, the present invention utilizes the selected active output of the decoder to set the other outputs to the inactive state. This also enables the decoder to reduce the loading on the input signals to only two gate loads and two drain loads as against four gate loads in the prior art.

We claim:

1. An improved binary decoder providing reduced size, reduced transistor count, increased speed, reduced input signal loading and increased speed of operation, comprising:
   - a selection means that activates a selected output corresponding to the input binary value, and
   - a deselecting means coupled to each output that deactivates all other outputs when the selected output is activated.

2. An improved binary decoder as claimed in claim 1, wherein the selection means is a circuit arrangement of gates for selecting a desired output.

3. An improved binary decoder as claimed in claim 1, wherein the deselecting means is a circuit arrangement having a single input connected to the desired output of the selection means, and a plurality of outputs each of which is connected to one of the remaining outputs of the selection means, such that when the input of the circuit arrangement is active all the other outputs of the decoder are forced to the inactive state.

4. A method for providing an improved binary decoder enabling reduced size, reduced transistor count, increased speed, reduced input signal loading and increased speed of operation, comprising the steps of:
   - providing a selection means for activating a selected output corresponding to the input binary value, and
   - providing a deselecting means coupled to each output for deactivating all other outputs when the selected output is activated.

5. An improved binary decoder providing reduced size, reduced transistor count, increased speed, reduced input signal loading and increased speed of operation substantially as herein described with reference to and as illustrated in figures 5 to 10 of the accompanying drawings.

6. A method for providing an improved binary decoder enabling reduced size, reduced transistor count, increased speed, reduced input signal loading and increased speed of operation substantially as herein described with reference to and as illustrated in figures 5 to 10 of the accompanying drawings.

Dated this 8th day of July, 2002

(ARCHANA SHANKER)
of **ANAND & ANAND, Advocates**
Agents for the Applicants

ABSTRACT

The present invention provides an improved binary decoder incorporating a selection circuit that activates a selected output corresponding to the input binary value, and a deselecting circuit coupled to each output that deactivates all other outputs when the selected output is activated. The deselecting circuit arrangement has a single input connected to the selected output and a plurality of outputs each of which is connected to one of the remaining outputs and forces them to the inactive state whenever the selected output is activated.

PRIOR ART

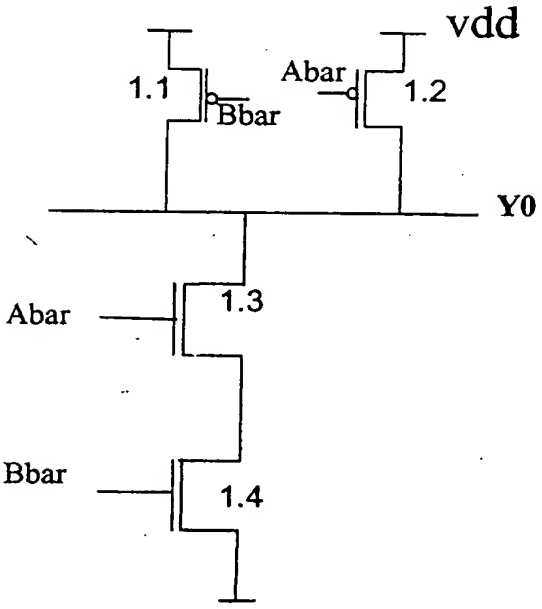

FIGURE 1

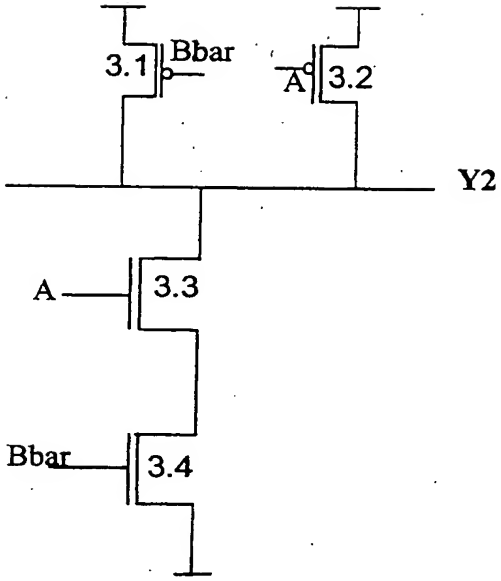

FIGURE 2

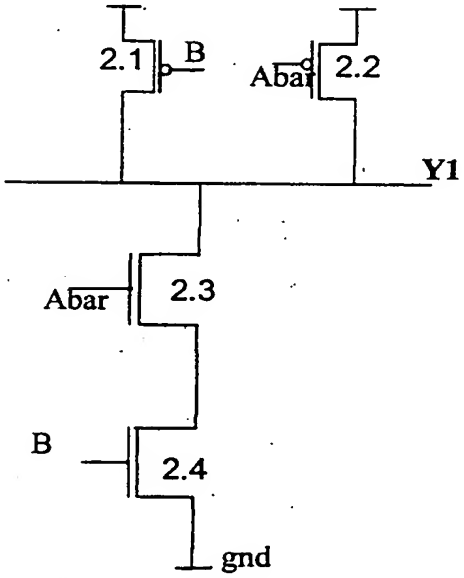

FIGURE 3

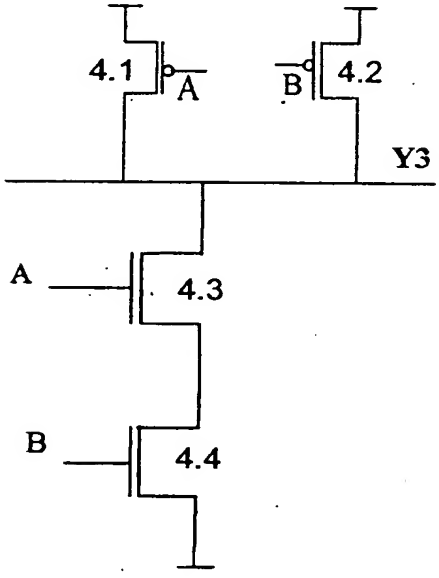

FIGURE 4

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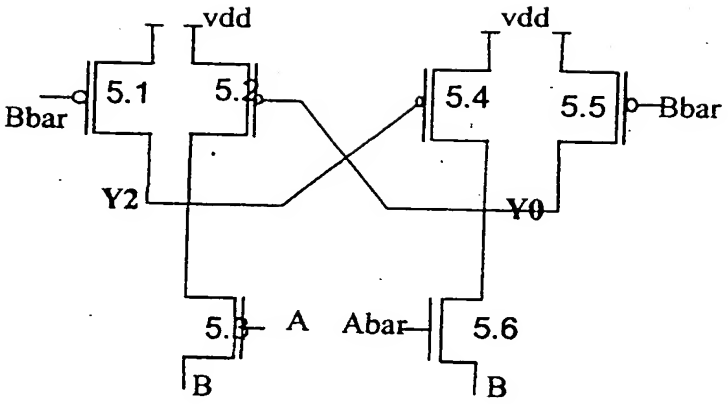

FIGURE 5

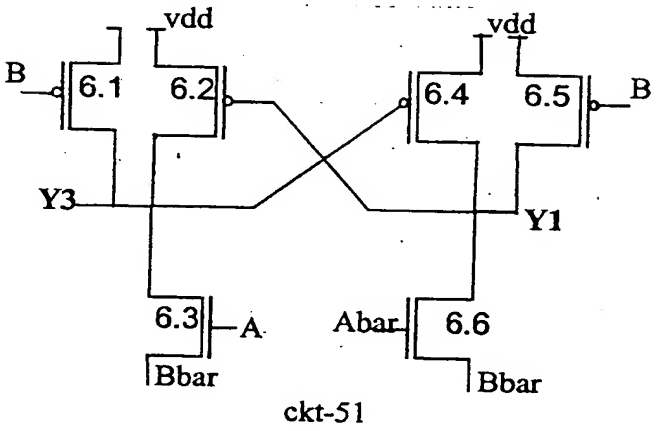

FIGURE 6

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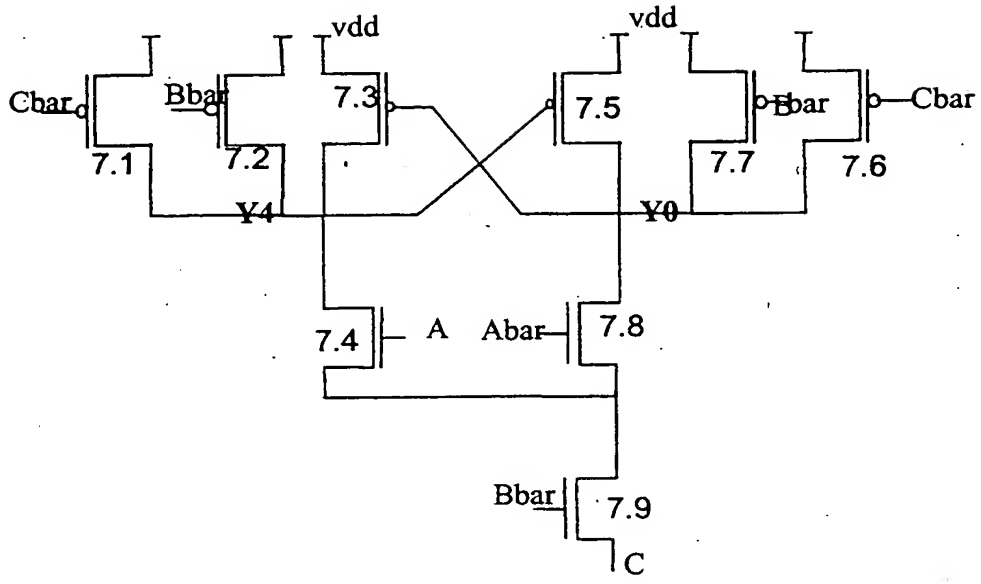

FIGURE 7

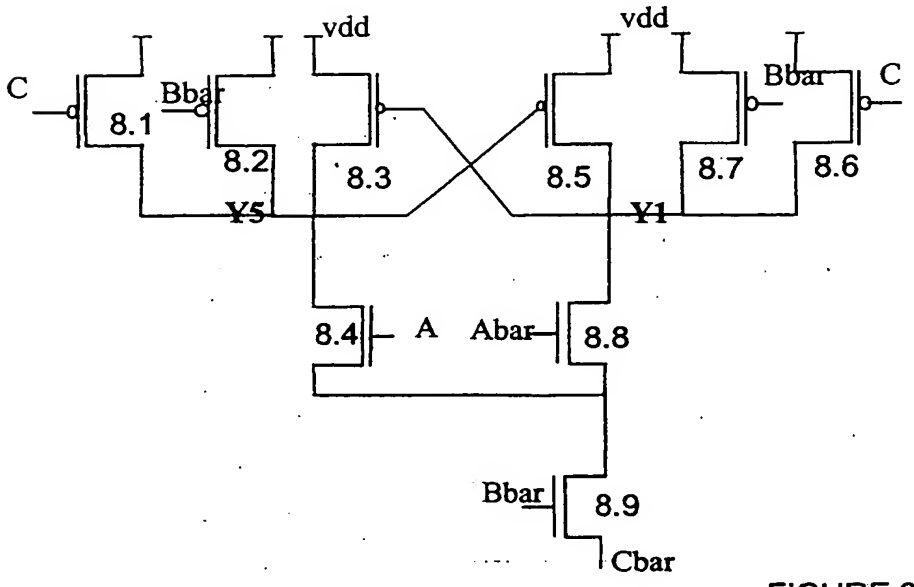

FIGURE 8

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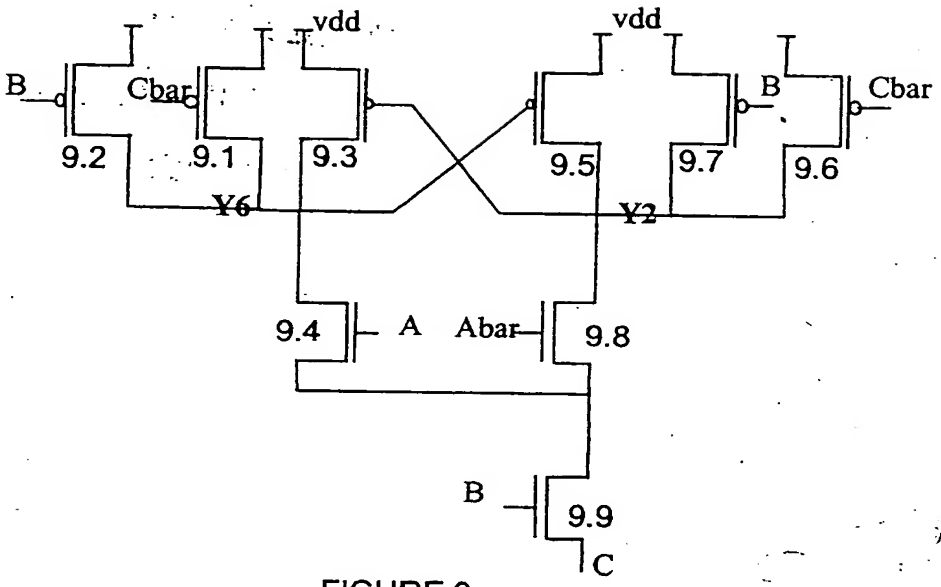

FIGURE 9

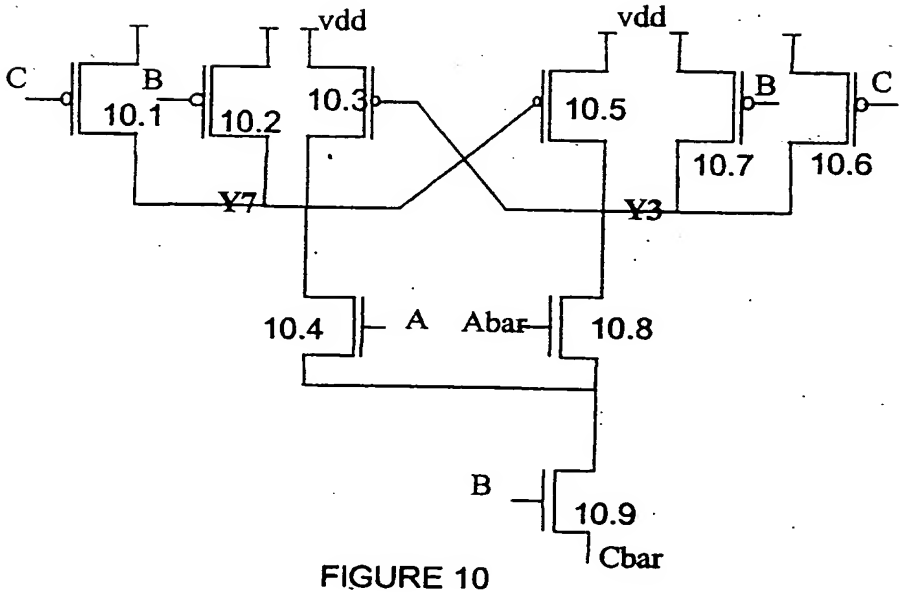

FIGURE 10

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